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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,898	04/02/2001	Eric B. Kushnick	CRED 2164	2197

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/824,898	KUSHNICK, ERIC B.	
	Examiner	Art Unit	
	Tse Chen	2116	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 30 December 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: _____.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

JOHN R. COTTINGHAM
PRIMARY EXAMINER

Continuation of 5. does NOT place the application in condition for allowance because of the following:
Applicant's arguments, with respect to pages 2-7 of Remarks, have been fully considered but they are not persuasive.
Regarding part 1, Examiner appreciates the careful scrutiny by Applicant to point out Examiner's inaccurate wording of "adjusted" in paragraph 34 of the Final Rejection. The more accurate statement should read "input period Tp is delayed by the number of N or M delay elements ..."
Regarding part 2, Applicant alleges that "the fact that Heyne's circuit brings the OUT signal into phase with the IN signal would somehow lead one of skill in the art to conclude that the delays of inverters I1 and I2 must be 'integer fractions of the period of [the IN] signal in order to have a practical apparatus that can incrementally adjust the delay circuit to achieve synchronization'" is incorrect and supports the allegation with parts 2a-2c.
Regarding part 2a, Applicant alleges that "one of skill in the art looking at Heyne's circuit schematic would not conclude that the delays of inverters I1 and I2 have any particular relationship to the period of the IN signal." Examiner kindly reminds Applicant that a circuit schematic alone may be insufficient to cover all aspects of an invention. If schematics were all that is necessary to describe all aspects of an invention, the whole database at the USPTO would be depicted in schematics without any accompanying written disclosure. What needs to be emphasized in this particular instance is that the reference has to be read as a whole and be interpreted through the eyes of one with ordinary skill in the art. As clearly demonstrated in parts 35-38 of the Final Rejection, one with ordinary skill in the art would have recognized that Heyne's apparatus does advocate the delay resolutions to be integer fractions of the period of an input signal in order to have a practical apparatus that can incrementally adjust the delay circuits to achieve synchronization.
Regarding part 2b, Applicant alleges that Heyne "provides no reason for one skilled in the art to conclude that the inverter delay is an integer fraction of the period of the IN signal, or indeed that it would have any particular relationship to the period of the IN signal." Applicant supports this allegation with a definition of resolution as applied by "one of ordinary skill in the electronic arts world" to demonstrate that Heyne's "OUT and IN would have the 'same' phase only to the extent that the Heyne's circuit is able to resolve its delay adjustment." However, Applicant did not make the necessary connection between the allegation and support. Instead, Applicant's demonstration can be seen to be in support of Examiner's position that the inverter delay elements I1 and I2 would necessarily have to be an integer fraction of the period of the IN signal in order for a practical synchronization circuit to be implemented. Specifically, in order to resolve the delay adjustment so that the OUT and IN would have the same phase [or as close to it as possible], the finest resolution, t1, would have to be an integer fraction of the IN period in order for a practical synchronization circuit to be implemented [parts 35-38 of the Final Rejection].
Regarding part 2c, Applicant alleges that the "most important reason the Examiner's assertion that Heyne's statement about bringing OUT into phase with IN teaches one of skill in the art that the inverter delays are Tp/M and Tp/N is incorrect is because Heyne directly teaches us the inverter delays are chosen on another basis." Applicant supports this allegation by pointing specifically to col.5, l.49 – col.6, l.2 of Heyne and asserts that Heyne indicates that the delays of inverters t1 and t2 should be chosen as functions of the maximum temperature dependent fluctuation range of the entire delay circuit, and teaches away from the notion that the delays of inverters t1 and t2 are or should be set to integer fractions of the period of the IN signal." Firstly, Heyne does not "teach away from the notion that the delays of inverters t1 and t2 are or should be set to integer fractions of the period of the IN signal." In order for Heyne to teach away from a limitation, Heyne has to specifically state or suggest that such limitation would be incompatible or undesirable with the invention. Applicant did not indicate where Heyne specifically stated or suggested that the inverter delays are not to be integer fractions of the IN period due to whatever reason. Secondly, Applicant is mistaken in concluding that because Heyne specifically teaches delay t2 should correspond to the maximum fluctuation range of the delay time due to temperature influences, then Heyne also teaches the negligence of other design criteria. The two teachings are not mutually exclusive: delay t2 may correspond to the maximum fluctuation range of the delay time due to temperature influences and still be set to an integer fraction of the IN period [note that Heyne teaches correspondence to a range, not equivalent to a specific value]. Surely, Applicant would not suggest that it would be correct for Examiner to conclude that because Applicant specifically teaches Tp/M and Tp/N to be integer fractions of Tp period, then Applicant also teaches the negligence of taking into consideration other design criteria such as temperature influence [i.e., temperature influence may affect operating performance in terms of generating delays that are not integer fractions of Tp period].
Regarding part 3, Applicant alleges that Heyne "clearly teaches that M and N are not relatively prime" by pointing specifically to figure 3 and col.5, l.49 – col.6, l.2 of Heyne. Applicant supports this allegation with a mathematical proof demonstrating that the ratio of t1/t2 can be used to derive the values for N[1] and M[4]. Examiner commends Applicant for this rather elegant demonstration of an important support. Alas, Applicant's proof only further strengthens Examiner's position because Applicant had erred in concluding that 1[N] and 4[M] are not relatively prime. According to standard math and Applicant's own disclosure, two numbers are relatively prime if they have no common factors other than 1. The factors of 4 are 1, 2, and 4 while the factor for 1 is 1. Therefore, the only common factor for 1[N] and 4[M] is 1, which means N and M are relatively prime.
Regarding part 4, Applicant alleges that Heyne does not suggest various delay ranges of Tp as stipulated in claim 4. Applicant's concession in the previous response concerning "while Heyne does not directly teach that the second delay unit has a delay as large as Tp one of skill in the art would expect it to have a delay that large" is important because it demonstrates one of the important aspects of Heyne's invention: the second delay unit is used to initially increment the number of second delay elements close enough to the desired phase and then held constant. Examiner also stated in part 42 of the Final Rejection which Applicant has conceded that the abstract which states "in the event of subsequent changes in the desired value or in the actual value, the number of first delay elements is incrementally altered, while the number of second delay elements in the signal path is kept constant, the first delay circuit, thus, would have to have a range that is at least as wide as (1-1/N)Tp in order to properly adjust the delay after initialization since the second delay elements are held constant and can't be used in the event that a full period Tp adjustment is desired. In essence, the relationship between the delay elements and Tp would have to be established in order for the synchronization operation to work properly. Therefore, letting the sum of all first delay elements be equivalent to Tp according to figure 3 would yield 12t1 which means the sum of all second delay elements would be 20t1 or 5/3 Tp. Applicant further attempts to support this allegation with a mathematical proof involving K and Dtemp. The proof is lacking in this case as it takes what was stated by Heyne and assumes that Heyne had taught against all other design criteria as discussed above. Thus, the conclusions derived from this proof would be fallacious.
As demonstrated above, Applicant's allegations, with respect to pages 2-7 of Remarks, are not persuasive and the rejections of all related limitations are maintained.

Applicant's arguments, with respect to Hondeghem in claims 1, 3, 4, 6, 15, 20, 22, 23, 25, 30, and 34, have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the instant case, Applicant concentrated the attack on Hondeghem when the rejection was based on a combination of Heyne and Hondeghem [e.g., Applicant is invited to reference parts 4-8 of the Final Rejection and note that Heyne and Hondeghem combined disclose each and every limitation of claim 1]. As to Applicant's allegation that "nothing anywhere in Hondeghem teachings anything about supplying repetitive first an second control data sequence as input to circuits having the nature and function of the first and second control means recited in the applicant's claims", Examiner invites Applicant to reference col.6, ll.20-57 of Hondeghem and note that the repetitive fashion is indeed taught [sequence 53 pulses 175 repeated 9434 times].

Applicant's arguments, with respect to claims 2, 5, 21, 24, 34, 7, 8, 16, 11, 26, 27, and 35, have been fully considered but they are not persuasive due to the reasons set forth above.

Applicant's arguments, with respect to Liedberg in claims 9-10, 12-14, 17-19, 28-29, 31-33, and 36-38, have been fully considered but they are not persuasive.

As discussed above, Applicant is reminded that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. In the instant case, Applicant concentrated the attack on Liedberg when the rejection was based on a combination of Liedberg and other references [note that Heyne discloses a set of gates and Liedberg discloses another set to complete the configuration].

As demonstrated above, Applicant's allegations, with respect to aforementioned claims, are not persuasive and the rejections of all related limitations are maintained.